AMENDMENTS TO THE CLAIMS:

Please cancel claims 4-8, 13, 16-24 and 31-47 without prejudice or disclaimer, add new claims 48-53, and amend the claims as follows:

1. (Currently Amended) A semiconductor device comprising a MIS type field effect transistor, wherein the transistor comprises: ~~comprising:~~

a silicon substrate;

a gate insulating film comprising a high-dielectric-constant metal oxide film and a silicon containing insulating film lying between the metal oxide film and the silicon substrate;

a silicon containing gate electrode formed on the gate insulating film, a gate length of said silicon containing gate electrode being not greater than 1μm; and

a sidewall including silicon oxide as a constituting material, which is formed on each lateral face side of the gate electrode; ~~and~~

wherein a silicon nitride film is interposed between the sidewall and at least the lateral face of the gate electrode, and

wherein the silicon nitride film covers the lateral face of the high-dielectric-constant metal oxide film, and a silicon oxide film underlies the silicon nitride film.

2. (Previously Presented) The semiconductor device comprising the MIS type field effect transistor according to Claim 1, wherein the silicon nitride film is laid between the sidewall and the silicon substrate.

3. (Withdrawn) The semiconductor device comprising the MIS type field effect transistor according to Claim 1, wherein the silicon nitride film is absent between the sidewall and the silicon substrate.

4-8. (Canceled)

9. (Previously Presented) The semiconductor device according to Claim 1, wherein a silicon nitride film is laid between the high-dielectric-constant metal oxide film and the gate electrode.

10. (Previously Presented) The semiconductor device according to Claim 1, wherein the high-dielectric-constant metal oxide film contains hafnium (Hf).

11. (Previously Presented) The semiconductor device according to Claim 1, wherein a dielectric constant of the high-dielectric-constant metal oxide film is not less than 10.

12. (Previously Presented) The semiconductor device according to Claim 1, wherein the high-dielectric-constant metal oxide film is absent beneath the sidewall.

13-24. (Canceled)

25. (Previously Presented) The semiconductor device according to Claim 1, wherein a thickness of the silicon oxide film is within a range of 1 to 20 nm.

26. (Previously Presented) The semiconductor device according to Claim 1, wherein a thickness of the silicon oxide film is within a range of 5 to 10 nm.

27. (Previously Presented) The semiconductor device according to Claim 1, wherein a thickness of the silicon nitride film is within a range of 1 to 10 nm.

28. (Withdrawn) The semiconductor device according to Claim 1, wherein the high-dielectric-constant metal oxide film has a nitridation region on each of its lateral face sides.

29. (Withdrawn) The semiconductor device according to Claim 1, wherein the nitridation region is formed within a range of 1 to 20 nm in the direction from its lateral face to inside of the gate electrode, and a nitrogen content in the region is not less than 5%.

30. (Withdrawn) The semiconductor device according to Claim 1, wherein the nitridation region is formed within a range of 1 to 20 nm in the direction from its lateral face to inside of the gate electrode, and a nitrogen content in the region is not less than 10%.

31-47. (Canceled)

48. (New) The semiconductor device according to claim 1, wherein said gate length is not greater than 200 nm.

49. (New) The semiconductor device according to claim 1, wherein said gate length is not greater than 100 nm.

50. (New) A semiconductor device comprising a MIS type field effect transistor, wherein the transistor comprises:

a silicon substrate;

a gate insulating film comprising a high-dielectric-constant metal oxide film and a silicon containing insulating film lying between the metal oxide film and the silicon substrate; and

a silicon containing gate electrode formed on the gate insulating film, a gate length of said silicon containing gate electrode being not greater than 1μm.

51. (New) The semiconductor device according to claim 50, wherein the transistor further comprises a silicon nitride film formed so as to cover a lateral face of the high-dielectric-constant metal oxide film.

52. (New) The semiconductor device according to claim 1, wherein said gate length is not greater than 200nm,

wherein a thickness of the silicon oxide film is with a range of 5 nm to 10 nm, and

wherein a thickness of the silicon nitride film is within a range of 1 nm to 10 nm.

53. (New) The semiconductor device according to claim 1, wherein said gate length is not greater than 100 nm,

wherein a thickness of the silicon oxide film is within a range of 5 nm to 10 nm, and

wherein a thickness of the silicon nitride film is within a range of 1 nm to 10 nm.